17. The FinFET structure of claim 16, wherein the second gate is positioned at a center portion of the substrate.

18. The FinFET structure of claim 17, wherein the center portion and the edge portion of the substrate each comprises both a dense gate region and an isolated gate region.

19. The FinFET structure of claim 15, wherein a difference between the lower width of the first gate in proximity to a bottom of the sidewall surface and the upper width of the first gate in proximity to the top surface of the semiconductor fin is below 15 nm.

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